

## METHOD FOR FORMING A BARRIER LAYER

### FIELD OF THE INVENTION

The present invention relates to the field of semiconductors  
5 and, more particularly, to an improved barrier layer for  
increasing semiconductor performance.

### CROSS-REFERENCES TO RELATED APPLICATIONS

This application is related to commonly assigned U.S. Patent  
10 Application Serial Nos.: \_\_/\_\_,\_\_ (Attorney Docket No.  
MIO0060PA), METHOD FOR FORMING A DIELECTRIC LAYER TO INCREASE  
SEMICONDUCTOR DEVICE PERFORMANCE, filed \_\_\_\_, by Powell et al.  
and \_\_/\_\_,\_\_ (Attorney Docket No. MIO0061), METHOD FOR FORMING  
A DIELECTRIC LAYER AT A LOW TEMPERATURE, filed \_\_\_\_, by Mercaldi  
15 et al., the disclosures of which are incorporated herein by  
reference.

### BACKGROUND OF THE INVENTION

There is a constant demand for semiconductor devices of a  
20 reduced size. The performance of semiconductor capacitors,  
transistors, electrode layers and the like in semiconductor  
devices becomes more critical as device size decreases.  
Accordingly, processes that result in increased device



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BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

The following detailed description of the present invention can be best understood when read in conjunction with the accompanying drawings, where like structure is indicated with like reference numerals.

Figure 1A illustrates a semiconductor device using a barrier layer according to one embodiment of the present invention.

Figure 1B illustrates a transistor semiconductor device utilizing a barrier layer according to one embodiment of the present invention.

Figure 2A is a flowchart of a method for fabricating a barrier layer according to another embodiment of the present invention.

Figure 2B illustrates exemplary thickness measurements of the barrier layer using the method of figure 2A.

Figure 3 illustrates capacitance characteristics of a semiconductor device utilizing a barrier layer according to another embodiment of the present invention.

Figure 4 illustrates a barrier layer according to another embodiment of the present invention.

Figure 5 is an illustration of a computer system for use with embodiments of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Figure 1A illustrates a semiconductor device 108 using a barrier layer 102 according to one embodiment of the present invention. The semiconductor device 108 is merely illustrated schematically in figure 1 and is typically fabricated proximate to a substrate 101. More specifically, the semiconductor device 108 may be formed in, on or over the substrate 101. For the purposes of defining and describing the present invention, it is noted that a semiconductor device 108 may comprise a transistor, capacitor, electrode, insulator or any of a variety of components commonly utilized in semiconductor structures. The substrate 101 may comprise one or more semiconductor layers or semiconductor structures which may define portions of the semiconductor device 108. The barrier layer 102 is formed over the semiconductor device 108. Generally, the barrier layer 102 is formed by depositing one or more precursor materials from a silane or silazane source and converting the deposited materials into the barrier layer 102 by subsequent processing of the deposited materials. The subsequent processing of the deposited materials involves subjecting the deposited materials to a reactive agent, such as an oxidizing or nitridizing species, which will react with silicon in the deposited materials. The barrier layer 102 reduces or prevents diffusion or migration of dopants into and

out of the semiconductor device 108 and reaction or oxidation of the materials forming the semiconductor device 108.

Figure 1B illustrates a transistor semiconductor device 109 utilizing a barrier layer 102 according to another embodiment of the present invention. A source 105 is formed in a substrate 101. A drain 106 is formed in the substrate 101. A gate oxide layer 104 is formed over the substrate 101 from the source 105 to the drain 106. A barrier layer 102 is formed over the gate oxide layer 104. An electrode or gate electrode 103 is formed over the barrier layer 102. The source 105, the drain 106, the substrate 101, the gate oxide layer 104 and the gate electrode 103 may be provided in accordance with convention techniques of semiconductor fabrication.

The barrier layer 102 is fabricated by vapor depositing one or more selected materials or precursors from a silicon source and subsequently processing those materials or precursors. The silicon source may be a silazane or a silane source such as hexamethyldisilazane (HMDS). Other silicon sources which may be used are tetramethyldisilazane, octamethylcyclotetrasilazine, hexamethylcyclotrisilazine, diethylaminotrimethylsilane or dimethylaminotrimethylsilane. The selected material is processed in a reactive ambient to create a final desirable silicon-containing barrier layer. Reactive ambients include oxygenating

or nitridating species which will react with silicon to form the silicon-containing barrier layer. Some reactive ambients are  $\text{NH}_3$ ,  $\text{N}_2$ ,  $\text{O}_2$ ,  $\text{O}_3$ ,  $\text{NO}$  and the like. The resulting silicon-containing barrier layer is the barrier layer 102 and may  
5 comprise a layer that is primarily nitride, primarily oxide or an oxynitride depending on the reactive ambient selected.

The barrier layer 102 prevents dopants, such as boron, in the gate electrode 103 from diffusing into the gate oxide layer 104, the source 105 and the drain 106. The barrier layer 102  
10 also prevents reactions between the gate electrode 103 and the gate oxide layer 104, prevents migration of dopants from the gate electrode 103 to other areas of the semiconductor device, prevents oxidation of the gate electrode 103 and prevents the formation of silicides on the gate electrode.

Figure 2A illustrates a method for fabricating a barrier  
15 layer according to one embodiment of the present invention. A wafer or substrate is provided at block 201. The wafer or substrate is cleaned using hydrofluoric acid (HF) at block 202. A silicon-containing material is vapor deposited onto the surface  
20 of the wafer at block 203 from a silicon source. The silicon-containing material is treated or processed using rapid thermal nitridation (RTN) in an  $\text{NH}_3$  ambient at block 204 resulting in creation of the barrier layer. The temperature, anneal time and

processing pressure are selected to obtain desired barrier layer characteristics. A wet oxidation layer is formed over the barrier layer at block 205.

Figure 2B illustrates thickness measurements of the barrier layer and wet oxidation layer created using the method of figure 2A using various processing conditions. In this figure, the wet oxidation has a thickness of 300Å. For this particular example, figure 2B illustrates that a suitable barrier layer may be formed at about 450 Torr and 850°C, over a processing time of 60 seconds with minimal oxidation of the underlying silicon substrate. It is noted that the 850°C processing temperature is lower than the processing temperature (typically 950°C) used to create barrier layers using conventional methods. In addition, the 60 seconds processing time is lower than the processing time used to create barrier layers using conventional methods (typically 45 minutes). However, the processing time can be longer without a detrimental affect if silane or silazane silicon sources are used because they are self limiting.

Generally, conventional barrier layers are processed using temperature ranges of 700°C to 1050°C, processing time of 10 seconds to 60 minutes, and processing pressure of 760 torr. Whereas, the barrier layer of the present invention is typically processed using temperature ranges of 500°C to 900°C, processing

time of 30 seconds to 5 minutes, and processing pressure of 450 torr. It is contemplated that variations to these ranges may also result in suitable barrier layer formation.

Referring to figures 1B and 3, figure 3 illustrates the capacitance characteristics of a semiconductor device 109 utilizing a barrier layer 102 according to the present invention. The capacitance characteristics of a device with a conventional barrier layer with a N+ PH<sub>3</sub> doped polysilicon gate electrode are illustrated at 301. Line 302 illustrates the capacitance characteristics of a device with a conventional barrier layer and a BF<sub>2</sub> doped polysilicon gate electrode. Line 303 shows the capacitance characteristics of a barrier layer 102 created by vapor depositing HMDS with a N+ PH<sub>3</sub> doped polysilicon gate electrode 103. Line 304 shows the capacitance characteristics of a device with a barrier layer 102 created by vapor depositing HMDS with a BF<sub>2</sub> doped polysilicon gate electrode. Comparing the capacitance values of lines 301 and 302 with lines 303 and 304, it is noted that negative bias capacitance is enhanced by the present invention. The barrier layers used in lines 303 and 304 were processed using NH<sub>3</sub> and O<sub>2</sub>.

In addition, line 302 shows how the conventional barrier layer suffers boron diffusion into the gate and active areas (note the shift in threshold voltage at 306). Line 307 shows

that the measured work function, associated with the vapor deposited HMDS barrier layers of lines 303 and 304 match theoretical values.

Figure 4 illustrates use of a barrier layer 402 according to another embodiment of the present invention. The barrier layer 402 is located between a dielectric 403 and a electrode 401. The barrier layer 402 is created by depositing a silicon-containing material (from silazane or silane type silicon sources). The layer is then post-processed in a reactive ambient. The dielectric 403 is of a material susceptible to oxygen migration such as  $Ta_2O_5$ . The electrode is of a material such as P-Si, SiGe, a metal, or any other electrode material suitable for use in semiconductor based charge storage devices.

Figure 5 is an illustration of a computer system 512 that can use and be used with embodiments of the present invention. As will be appreciated by those skilled in the art, the computer system 512 would include ROM 514, mass memory 516, peripheral devices 518, and I/O devices 520 in communication with a microprocessor 522 via a data bus 524 or another suitable data communication path. The mass memory 516 can include silicon-containing barrier layers in, for example, transistor structures or charge storage structures. These devices can be fabricated according with the various embodiments of the present invention.

For the purposes of describing and defining the present invention, formation of a material "on" a substrate or layer refers to formation in contact with a surface of the substrate or layer. Formation "over" a substrate or layer refers to formation either above or in contact with a surface of the substrate.

As stated earlier, barrier layers fabricated using the present invention can be used for a variety of purposes. Some examples follow, but embodiments of the present invention are not limited to these. A barrier layer can be formed on top of metals to prevent oxidation of metals. A barrier layer can be placed between metals and silicon containing materials to prevent agglomeration, the formation of silicides. A barrier layer can be used in a P+ or N+ gate to prevent dopant, hydrogen, or fluorine in-diffusion into the gate dielectric reducing defect density and increasing performance and reliability. A barrier layer can be used in post gate stack and pre oxidation steps to prevent oxygen in-diffusion into active areas of the transistor. A barrier layer can be used to prevent oxidation of gate electrodes with subsequent processing steps when using materials such as polysilicon, Si-Ge, W or other transition metals. A barrier layer can be used with a storage dielectric, such as non-volatile random access memory, and may be used to reduce degradation of tunnel oxide performance.

Having described the present invention in detail and by  
reference to preferred embodiments thereof, it will be apparent  
that modifications and variations are possible without departing  
from the scope of the present invention defined in the appended  
5 claims.